Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently amended) A two-transistor DRAM cell consisting:

an NMOS device with a first gate adapted to couple with write word line, a first controlled node adapted to couple with write bit line, and a second controlled node;

a PMOS device with a second gate, a third controlled node adapted to couple with a read word line, and a fourth controlled node adapted to couple with read bit line, the second gate of the PMOS device coupled to the second controlled node of the NMOS device; and

a storage node coupled to the second gate of the PMOS device and the second controlled node of the NMOS device, wherein the NMOS and PMOS devices are adapted to provide to the storage node a capacitance equal to a sum of parasitic capacitances of the second controlled node of the NMOS device and the second gate of the PMOS device.

2. (Currently amended) The two-transistor DRAM cell of claim 1, wherein the ~~storage node is defined between the PMOS device and the NMOS device, the~~ storage node having a voltage that converges to Vhigh, where Vhigh is greater than Vcc/2.

3.-10. (Cancelled)

11. (Currently amended) A two-transistor DRAM cell consisting:

a read bit line;

a write bit line;

a read word line;

a write word line;

an NMOS device with a first gate region coupled to the write word line, a first controlled node region coupled to the write bit line, and a second controlled node region;

a PMOS device with a second gate region, a third controlled node region coupled to the read word line, and a fourth controlled node region coupled to the read bit line, the second gate region of the PMOS device coupled to the second controlled node region of the NMOS device; and

a storage node coupled to the second gate region of the PMOS device and the second control node region of the NMOS device, wherein the NMOS and PMOS devices are adapted to provide to the storage node a capacitance equal to a sum of parasitic capacitances of the second controlled node of the NMOS device and the second gate of the PMOS device.~~a p-channel (PMOS) device coupled between the read bit line and the read word line; and~~

~~an n-channel (NMOS) device coupled between the write bit line and a gate region of the PMOS device so as to form a storage node therebetween~~.

12.-13. (Cancelled)

14. (Currently amended) The DRAM cell of claim 11~~13~~, wherein the write word line is pulled from a logic low voltage to a logic high voltage to write data into the DRAM cell.

15. (Currently amended) The DRAM cell of claim 11~~13~~, wherein the read word line, the read bit line and the write word line are held at a logic low voltage to hold data within the DRAM cell.

16. (Currently amended) The DRAM cell of claim 11~~13~~, wherein the data written into the DRAM cell corresponds to the voltage level of the write bit line.

17. (Original) The DRAM cell of claim 11, wherein a voltage level of the storage node converges to logic high due to edge leakage current.

18.-20. (Cancelled)

21. (Currently amended) A system comprising:

an integrated circuit (IC); and

memory coupled to the IC, the memory including at least one two-transistor DRAM cell consisting

an NMOS device with a first gate coupled to a write word line, a first controlled node coupled to a write bit line, and a second controlled node;

a PMOS device with a second gate, a third controlled node coupled to a read word line, and a fourth controlled node coupled to a read bit line, the second gate of the PMOS device coupled to the second controlled node of the NMOS device; and

a storage node coupled to the second gate of the PMOS device and the second controlled node of the NMOS device, wherein the NMOS and PMOS devices are adapted to provide to the storage node a capacitance equal to a sum of parasitic capacitances of the second controlled node of the NMOS device and the second gate of the PMOS device.

22. (Original) The system according to claim 21, wherein the IC comprises a central processing unit, and at least one input/output module coupled to the central processor unit.

23. (Original) The system of claim 21, wherein the memory is coupled to the IC via the communication channel.